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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,196	11/20/2001	Chih-Chien Liu	UMC-96-279 CON2	3908
25235 7590 01/03/2007 HOGAN & HARTSON LLP ONE TABOR CENTER, SUITE 1500 1200 SEVENTEENTH ST DENVER, CO 80202			EXAMINER SERGEANT, RABON A	
			ART UNIT 1711	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE			MAIL DATE	
3 MONTHS			01/03/2007	
			DELIVERY MODE PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

09/991,196

Applicant(s)

LIU ET AL.

Examiner

Rabon Sergent

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to-communication(s) filed on 16 October 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-35 and 37-58 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 21-35 and 37-58 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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1. A request for continued examination under 37 CFR 1.114 was filed in this application after appeal to the Board of Patent Appeals and Interferences, but prior to a decision on the appeal. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on October 16, 2006 has been entered.

2. Claims 45 and 57 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Firstly, the language, "high temperature step", is subjective, because it is unclear what quantitative values are encompassed by "high".

Secondly, it is unclear from the language, "high temperature step", what step or operation is encompassed by the language. It is by no means clear that the language would be interpreted in the same manner by one of ordinary skill as argued by applicant within pages 9 and 10 of the response.

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference

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claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 21-35 and 37-58 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-32 of copending Application No. 11/315,904. Although the conflicting claims are not identical, they are not patentably distinct from each other because each set of claims is drawn to a method of forming conducting structures separated by gaps, wherein a layered structure comprising a substrate having a wiring line layer, a cap layer, and a mask layer is etched to produce the wiring lines separated by gaps; the gaps are then filled with dielectric material by such means as high density plasma chemical vapor deposition.

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This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 21-23, 28-35, 37-39, 45-53, and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 8-288285 in view of Tobben et al. ('126).

JP 8-288285 discloses a process for forming wiring line layers on a substrate by etching, wherein the substrate has upon it a wiring line layer, a protection insulating film corresponding to applicants' claimed cap layer (see layer 4 within figures and page 9, lines 1-6 of translation), and a resist mask, corresponding to applicants' claimed mask layer (see layer 6 within figures and page 12, line 18 of translation). The reference further discloses steps wherein the mask layer is patterned, the cap layer is etched according to the mask layer pattern, the mask layer is removed, and the wiring line is etched according to cap layer pattern. See page 12, line 11

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through page 14 line 10 of the translation. The reference further discloses that after the wiring lines are formed, a planarized insulating film is applied by bias ECR plasma CVD. See page 14, lines 11-24 of the translation. The position is taken that the disclosed insulating film corresponds to applicants' claimed dielectric material and that in the course of applying the planarized film, the gaps between the wiring lines are inherently filled with dielectric material. Furthermore, the reference discloses at page 11, lines 11-16 of the translation that a high density plasma is generated by bias ECR plasma CVD; therefore, this CVD method is considered to meet applicants' claimed high density plasma chemical vapor deposition method. With respect to claims 49 and 53, it is noted that the reference teaches the use of inductively coupled plasma CVD and helicon wave plasma CVD within paragraph [0046] of the translation. With respect to claim 45, it is noted that the reference allows for the application of additional insulating layers (see paragraph [0046] of the translation) and that there is no specifically recited requirement for a high temperature heating step. Furthermore, applicants have failed to equate the disclosed act of annealing to the claimed high temperature heating step. Lastly, it appears that paragraph [0046] of the translation allows for the use of CVD equipment that, according to applicants, deposits material densely that does not require a separate step of densification.

7. The primary reference differs from the instant claims primarily in that while the primary reference discloses that an antireflection layer corresponding to applicants' conductive protective layer can be used as a cap layer (see translation paragraphs [0007] and [0045]), the primary reference fails to disclose the use of both the antireflection layer and a cap layer. It is noted that the translation discloses at paragraph [0044] that the invention of the reference is not limited to the embodiments; therefore, the reference is not considered to preclude modifications. Bearing

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this in mind, the position is taken that semiconductor structures having applicants' claimed layer structure of wiring line layer, conductive protective layer (antireflection layer), and cap layer were known at the time of invention. This position is supported by the teachings of Tobben et al. See figures; column 2, lines 32-46; and column 3, lines 6+. Therefore, the position is taken that it would have been obvious to incorporate the claimed conductive protective layer between the wiring line layer and the cap layer of the primary reference in accordance with the teachings of the secondary reference, so as to realize such advantages as increased protection of the wiring lines conveyed by the use of such a layer.

8. Applicants have argued that the method of JP 8-288285 fails to produce an initial structure, corresponding to figure 3 of the instant application. The examiner has carefully considered this argument; however, the argument is insufficient to overcome the prior art rejection for the following reasons. Despite applicants' remarks, it is not seen that applicants have conclusively established that the argued structure is not formed as some initial point of the deposition step of the reference. Applicants have provided no evidence that the disclosed process does not cause the argued structure to initially form, then as the process continues, the argued layers are removed. Applicants have not challenged that the deposition methods (i.e.; HDPCVD) of the instant claims and the prior art are the same or analogous; therefore, despite applicants' arguments, it remains unclear why different structures would be expected to result. Furthermore, within page 11 of the response, applicants state, "the '285 publication describes filling the gaps between wiring lines using a sufficiently high sputtering component to remove the deposited oxide from the sides of its protection insulating film patterns 4a and from the sides of the openings in the metal layer". Therefore, applicants' statement indicates that oxide has

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been initially deposited on the very surfaces that applicants argue are not initially coated by the deposition method of the reference. It stands to reason that for something to be removed, it must have initially been deposited. Applicants' arguments are therefore contradictory and cannot be afforded great weight.

9. Applicants have further argued that the planarization layer 16 of Tobben et al. cannot act as the cap layer defined in the pending claims. The examiner has considered this argument; however, the argument fails to adequately explain layer 16b of the prior art, which is disclosed as being a cap layer and appears from figure 2A to be relatively uniform in thickness.

10. Claims 24-27, 40-44, and 54-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 8-288285 in view of Tobben et al. ('126) as applied to claims 21-23, 28-35, 37-39, 45-53, and 58 above, and further in view of Muraoka et al. ('005) or Haraguchi et al. ('989) or Wakabayashi et al. ('640).

As aforementioned, the position is taken that the combined teachings of JP 8-288285 and Tobben et al. render applicants' claimed methods of depositing dielectric material between wiring line gaps *prima facie* obvious. Furthermore, the remarks, above within paragraph 6, with respect to claims 45, 49, and 53 also apply to claims 41 and 57. However, these references fail to disclose the modification of the cap layer to yield the claimed profiles of the cap layer prior to "depositing". However, it was known at the time of invention to utilize etching techniques to produce specific profiles, such as trapezoidal profiles, in the production of semiconductor articles and structures. See Haraguchi et al. as well as the figures of Muraoka et al. and Wakabayashi et al. Therefore, the position is taken that the use of etching to produce other than rectangular profiles or cross-sections within semiconductors was conventional at the time of invention and

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that such modifications amount to design choices that would have been obvious to one of ordinary skill at the time of invention.

11. The rejection of claims 24-27, 40-44, and 54-57 has been modified in response to applicants' arguments.

Any inquiry concerning this communication should be directed to R. Sergent at telephone number (571) 272-1079.

R. Sergent
December 22, 2006


RABON SERGENT
PRIMARY EXAMINER